

Exhibit 32

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

EMC CORPORATION,

Petitioner

v.

ACQIS LLC,

Patent Owner

Case No. IPR2014-01469

Patent: RE42,814

PATENT OWNER'S PRELIMINARY RESPONSE

UNDER 37 C.F.R. § 42.107

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Patent Trial and Appeal Board
U.S. Patent and Trademark Office
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List of Exhibits Cited in this Preliminary Response

- Exhibit 2001: *PCI Local Bus Specification*, Production Version, Rev. 2.1, June 1, 1995 (“PCI Local Bus Specification”)
- Exhibit 2002: *Computer Desktop Encyclopedia*, (2d Ed. 1999) (“Computer Desktop Encyclopedia”)
- Exhibit 2003: *Microsoft Press Computer Dictionary*, (3d Ed. 1997).
- Exhibit 2004: CERN DOCUMENT SERVER, Listing for Bogaerts, A. et al., *RD24 status report: application of the scalable coherent interface to data acquisition at LHC*, <http://cds.cern.ch/record/294145/files/>.
- Exhibit 2005: CERN LIBRARY RESOURCES, <http://library.web.cern.ch/resources>.
- Exhibit 2006: P.R. 4-3 Joint Claim Construction Statement, *ACQIS v. EMC Corp.*, 6:13-cv-00638-LED (E.D. Tex. Nov. 25, 2014)

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I. INTRODUCTION

Petitioner alleges that claims 24, 31, 32, and 33 of the '814 patent (“Petitioned Claims”) are unpatentable, asserting 6 grounds. The allegations rely on (1) for Grounds 1-6, a flawed construction of “PCI bus transaction” that ignores the language of the claims and the intrinsic record; (2) for Grounds 3-6, an alleged prior art reference—the Bogaerts Draft—that fails to meet the requirements of a printed publication under § 102(b); and (3) for Grounds 1-6, a scattershot presentation of prior art references allegedly combinable in 16 ways—none of which Petitioner provides proper explanation for. For these reasons, Petitioner fails to show that there is a reasonable likelihood that it will prevail as to at least one of the challenged claims. The Petition should be denied in its entirety.

All of the asserted grounds rely extensively on a flawed construction of “PCI bus transaction.” Petitioner proposes an unreasonably broad construction of “PCI bus transaction” that reads out the express definition of “PCI.”¹ As a consequence, Petitioner asserts art in Grounds 1-6 relevant to its flawed, overbroad construction

¹ In the related district court litigation, Petitioner agrees that “PCI bus transaction” should include “PCI” and cites the specification, prosecution history, and extrinsic evidence to support its position there. (Ex. 2006, at 3-8.) Here, however, Petitioner ignores all of that evidence in pursuit of its extreme position.

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but not to a proper construction consistent with the claim language. Under the proper construction of “PCI bus transaction,” each of the asserted grounds fails and institution should be denied.

Grounds 3-6 rely on an internal CERN draft document (the Bogaerts Draft) that does not qualify as a prior art printed publication. The title page of the Bogaerts Draft indicates that the document was just a preliminary draft. And the only date on the document suggests when the document was last edited or prepared, not when it was published, indexed, or posted publicly. Indeed, evidence from the CERN library indicates that CERN did not make the Bogaerts Draft accessible until 2008, well after the ’814 patent was filed. Petitioner simply submitted no evidence to establish an actual publication date of the draft document. Petitioner, for example, did not submit testimony from any one with knowledge of the Bogaerts Draft’s publication or offer any explanation for when it first could have been publicly accessible. The Bogaerts Draft is not a prior art publication, and Grounds 3-6 should be denied.

Grounds 1-6 against particular claims should also be denied because Petitioner fails to provide the necessary rationale for the combinations of those grounds. Petitioner has the burden to state the precise relief it requests and to specify how each claim is rendered unpatentable by the prior art. *See* 37 C.F.R. § 42.22(a); 37 C.F.R. § 42.104. In specifying how the cited art renders claims

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obvious, Petitioner must specify the precise combinations it asserts. *See Edmund Optics, Inc. v. Semrock, Inc.*, IPR2014-00583, Paper 9, at 10-12 (PTAB Sept. 19, 2014) (denying institution because petitioner offered combinations of references in the alternative). Petitioner fails to meet its burden by asserting combinations of Grounds 1-6 in the alternative. In all, Petitioner asserts seven different references for Grounds 1-6 resulting in 16 alternative combinations. Petitioner fails to meet its burden by also failing to explain how the references would actually be combined, leaving the Board and the Patent Owner to guess at Petitioner's positions.

As a result, Petitioner lacks the required specificity for the following Grounds:

- Ground 1 for claims 24 and 32
- Ground 2 for claim 32
- Ground 3 for all Petitioned Claims
- Grounds 4-6 for all Petitioned Claims

Without sufficient explanation for the combinations, institution on each of the obviousness grounds in Grounds 1-6 should be denied as to the above claims. *See Apple Inc. v. Achates Reference Publishing, Inc.*, IPR2013-00081, Paper 21, at 20-21 (PTAB June 3, 2013) (refusing to consider alternative combinations); *Wowza Media Systems, LLC v. Adobe Systems Inc.*, IPR2013-00054, Paper 12, at

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10-11 (PTAB Apr. 8, 2013) (refusing to consider undeveloped unpatentability theories).

II. GROUNDS 1-6 RELY ON PETITIONER’S FLAWED CLAIM CONSTRUCTION OF “PCI BUS TRANSACTION” AND SHOULD BE REJECTED

“PCI bus transaction” is recited in independent claims 24 and 31, from which all other Petitioned Claims depend. Claim 24 recites “two unidirectional serial channels that transmit encoded data of Peripheral Component Interconnect (PCI) bus transaction in opposite directions” and “a second LVDS channel comprising two unidirectional serial channels that transmit data in opposite directions, said second LVDS channel extending from said north bridge to convey said address and data bits of PCI bus transaction in serial form.” (Ex. 1001, at 27:23-26, 27:34-38.) Claim 31 recites “a peripheral bridge coupled to said microprocessor unit without any intervening Peripheral Component Interconnect (PCI) bus, said peripheral bridge coupled to said second LVDS channel to communicate address and data bits of PCI bus transaction in serial form over said second LVDS channel.” (Ex. 1001, at 28:34-39.)

The BRI of “PCI bus transaction” is “command, address, and data information, in accordance with the PCI standard, for communication with an interconnected peripheral component.” This construction is supported by both intrinsic evidence and extrinsic evidence. In contrast, Petitioner proposes that

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“PCI bus transaction” be construed as a generic bus transaction: “a digital signal communication with an interconnected peripheral component.” (Petition, at 13.)

Petitioner’s construction is unreasonably broad, ignoring the definition of “PCI” in the claims and other crucial evidence. As a consequence, Petitioner applies the cited art using a flawed interpretation of the claims for all of the asserted grounds and institution of all of the grounds should be denied.

Table 1 – Proposed constructions for “PCI Bus transaction”

Patent Owner’s Construction	Petitioner’s Construction
command, address, and data information, in accordance with the PCI standard, for communication with an interconnected peripheral component	a digital signal communication with an interconnected peripheral component

A. Patent Owner’s BRI Is Consistent With the Evidence

Patent Owner’s proposed construction is consistent with the plain and ordinary meaning of “PCI” and is properly supported by intrinsic and extrinsic evidence.

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1. “PCI bus transaction” is properly limited to bus transactions according to the Peripheral Component Interconnect protocol

A “PCI bus transaction” cannot reasonably be broader than a bus transaction of the Peripheral Component Interconnect protocol standard. The claims themselves limit “PCI” by expressly defining it to have its plain and ordinary meaning, “Peripheral Component Interconnect.” (Ex. 1001, at 27:23-26, 28:34-39.) By virtue of the express definition of “PCI” in the claims, it must be narrower than some generic transaction to any interconnected device.

The Board previously has found that industry acronyms like “PCI” should be given their plain and ordinary meaning, which is the phrase the acronym represents. For example, in *Ex Parte Li Chen*, the Board rejected an examiner’s BRI of “URL” as a generic “identifier” and found that the interpretation of “URL” should be limited specifically to “Uniform Resource Locator,” its plain and ordinary meaning. *Ex Parte Li Chen*, Appeal 2011-013075, at 2 (PTAB Jan. 22, 2014). According to the Board, the examiner’s interpretation was unreasonably broad. *Id.* (“Appellants contend ‘[the Examiner’s] asserted interpretation of the term “URL” is improper because the asserted interpretation is too broad and is not reasonable.’ Appellants contend that ‘URL’ has an established plain meaning in the computer arts. We agree with Appellants.” (citations omitted)).

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The Federal Circuit also interprets well-known industry acronyms according to their plain and ordinary meaning, even where the specification includes support for conflicting interpretations. In *Azure Networks, LLC v. CSR PLC*, the Federal Circuit recently interpreted “MAC address” according to its plain and ordinary meaning—“Media Access Control.” *Azure Networks, LLC v. CSR PLC*, No. 2013-1459, 2014 WL 5741337, at *10 (Fed. Cir. Nov. 6, 2014). Construing “MAC address” as “Media Access Control address” was appropriate in spite of statements in the specification that would suggest a meaning of “MAC” that differed from the industry-understood meaning of “Media Access Control.” *Id.* at *10-11 (finding that patentee’s reference to “Media Access (MAC) address” rather than “Media Access Control” “did not re-coin an established term”).

The Board similarly should limit “PCI” to the “Peripheral Component Interconnect” protocol standard and “PCI bus transaction” to a bus transaction according to that protocol standard. As stated in the claims, “PCI” stands for “Peripheral Component Interconnect” and should be interpreted as such. To attribute some meaning to “PCI bus transaction” broader than a bus transaction in accordance with the Peripheral Component Interconnect protocol, the specification must deliberately, clearly, and precisely set forth the broader meaning. *Azure Networks*, 2014 WL 5741337, at *10.

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Likewise, “Peripheral Component Interconnect” carries significant meaning as a proper noun beyond a generic interconnect for a peripheral component. The claims purposefully capitalize the term “Peripheral Component Interconnect.” “PCI bus transaction” should be interpreted no broader than the meaning of the proper noun “Peripheral Component Interconnect.” *See Fidelity National Information Services, Inc. v. Checkfree Corp.*, CBM2013-00030, Paper 16, at 8 (PTAB Dec. 23, 2013) (finding that “Automated Clearing House” is a proper noun specifically referring to the Federal Reserve ACH network, not a broader clearing house).

Extrinsic evidence further supports interpreting “PCI bus transaction” as a bus transaction specific to the Peripheral Component Interconnect, or PCI, protocol standard. In particular, the acronym “PCI” is consistently defined and described as relating to the PCI protocol. In one example, the *Computer Desktop Encyclopedia*, from 1999, defines “PCI” as “(Peripheral Component Interconnect) A peripheral bus commonly used in PCs, Macintoshes and workstations. It was designed primarily by Intel and first appeared in PCs in late 1993.” (Ex. 2002, at 6-7.) In another example, the *Microsoft Press Computer Dictionary*, dated 1997, defines a “PCI local bus” as relating to the PCI protocol, stating that it is “short for Peripheral Component Interconnect local bus. A specification introduced by Intel Corporation that defines a local bus system....” (Ex. 2003, at 7-8.) The consistent

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treatment “PCI” receives from extrinsic evidence shows that the BRI for “PCI bus transaction” should refer to a bus transaction according to the PCI protocol standard.

Next, Patent Owner’s BRI is consistent with the specification of the ’814 patent. In addition to the recited definition of “PCI” in the claims, the specification describes PCI “bus transactions” generated according to the PCI protocol standard and serialized for transmission over a low-voltage differential signal channel. Indeed, one of the goals of the invention is to serialize PCI protocol standard signals specifically, not some generic signal or alternative:

Embodiments in accordance with the present invention may interface two PCI or PCI-like buses using a non-PCI or non-PCI-like channel. In accordance with embodiments of the present invention, PCI control signals are encoded into control bits and the control bits, rather than the control signals that they represent, are transmitted on the interface channel. At the receiving end, the control bits representing control signals are decoded back into PCI control signals prior to being transmitted to the intended PCI bus.

(Ex. 1001, at 19:31-39.)

Lastly, Petitioner agrees in the related district court litigation that “PCI” refers to the industry standard PCI bus, a construction at odds with the one it

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presents here. (Ex. 2006, at 1, 3.) Indeed, both parties’ proposed constructions of “PCI” and “PCI bus transaction” in the district court define “PCI” as the PCI protocol standard. Patent Owner’s proposed constructions here and in the district court are the same. (*Id.*) In the district court, Petitioner proposes that “PCI bus transaction” means “signals communicated over a ‘PCI bus’” and “PCI bus” means an “industry standard computer bus known as the Peripheral Component Interconnect Local Bus.” (*Id.*) Thus, while the parties’ definitions differ to some extent in the district court, there is no dispute that a PCI bus transaction is a transaction according to the protocol set forth in the PCI standard.

Here, Petitioner’s proposed construction of “PCI bus transaction” reads “PCI” out of all of the Petitioned Claims. As a result, Petitioner applies the asserted art to every claim in all of the asserted grounds using a flawed interpretation of “PCI bus transaction.” For example, in Ground 1, Petitioner points to a generic serial bus and several bus protocols that are not PCI, including PCMCIA, INTEL serial bus, and IEEE P.1394, to meet the limitation. (Petition, at 20-21.) For Ground 2, Petitioner identifies a Tandem Computers proprietary bus (TNet) that carries proprietary bus transactions unrelated to PCI. (Petition, at 31-33.) Petitioner articulates its grounds through the prism of its generic and overbroad interpretation of “PCI bus transaction,” ignoring the PCI requirement. Petitioner’s failure to include “PCI” in its proposed construction combined with its

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failure to address the proper construction is fatal to all of Grounds 1-6. *See Superior Communications, Inc. v. Speculative Product Design, LLC*, IPR2013-00626, Paper 18, at 6, 10-11 (PTAB) (denying institution after interpreting term narrowly and finding that Petitioner failed to address the narrow interpretation.)

2. The broadest reasonable interpretation of “PCI bus transaction” includes the address, data, and command information from the Peripheral Component Interconnect protocol

Details provided in the specification about the PCI signals make clear that the bus transactions are specific to the PCI protocol and that each bus transaction includes specific information. The BRI of “PCI bus transaction” must be one that takes into account that specific information required by the PCI protocol.

According to the '814 patent, the specific information required by the PCI protocol includes “command, address, and data information.” Figure 10 in the '814 patent relates to a PCI bus transaction and illustrates the required command, address, and data information portions of a PCI bus transaction. In describing Figure 10, the specification states that the “[t]ransmitter 1230 receives multiplexed parallel address/data (A/D) bits and control bits from translator 1220 on the AD[31::0] out and the CNTL out lines, respectively.” (Ex. 1001, at 21:51-53.)

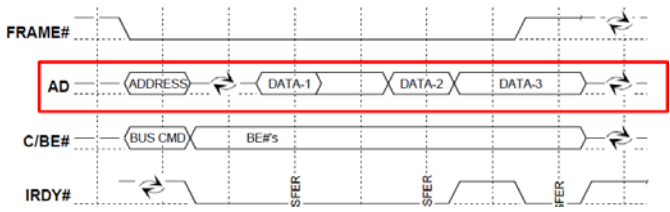
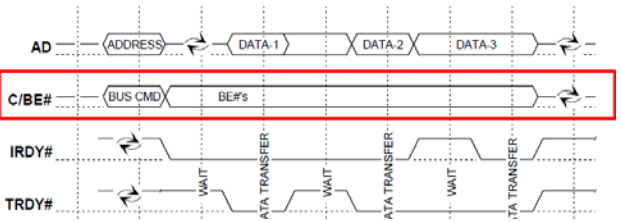
The specification’s description of the address, data, and control bits mirrors the PCI bus transaction as explained in the PCI Local Bus Specification, which is

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cited on the face of the '814 patent. In its section entitled “Bus Transactions” (Ex. 2001, at 51-55), it describes a PCI bus transaction as having an address phase and data phase “AD[31::00]” and a command, or control, phase “C/BE[3::0]#.” (Ex. 2001, at 52.)

The following table provides a side-by-side comparison of the disclosure of the '814 patent and the PCI Local Bus Specification.

Table 2 – Comparison of PCI bus transactions from the specification and the PCI Local Bus Specification

PCI Bus Transaction	
The '814 Patent (Ex. 1001, at 21:51-63 (bold added))	PCI Local Bus Specification (Ex. 2001, at 25, 52 (bold and annotations added))
address/data (A/D) bits . . . on the AD[31::0] out [line] . . .	<p>AD[31::00] . . . <i>Address and Data</i> are multiplexed . . .</p> 
and control bits . . . on the . . . the CNTL out lines	<p>C/BE[3::0]# . . . <i>Bus Command and Byte Enables</i> are multiplexed . . .</p> 

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The specification and other intrinsic evidence all consistently require a “bus transaction” of the PCI protocol to require “command, address, and data information.” The BRI of “PCI bus transaction” should not be no broader than that requirement.

In short, each of the claims, the description in the specification, and the cited art on the face of the patent uniformly suggest that “PCI bus transaction” should be construed consistent with Patent Owner’s BRI of “command, address, and data information, in accordance with the PCI standard, for communication with an interconnected peripheral component.”

B. Petitioner’s BRI Is Unreasonably Broad

Petitioner argues that “PCI bus transaction” should be construed as “a digital signal communication with an interconnected peripheral component,” the same construction applied by the district court in an earlier case. (Petition, at 13.) Petitioner’s proposed construction is flawed because (1) it ignores the express definition of “PCI” in the claims and (2) it ignores all other evidence aside from a single *Markman* order, an order Petitioner *agrees* was incorrectly decided. (Ex. 2006, at 1, 3-8)

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1. Petitioner’s unreasonably broad construction is inconsistent with the specification

Petitioner’s construction of “a digital signal communication with an interconnected peripheral component” ignores the express definition of “PCI” in the claims that limit a “PCI bus transaction” to a “Peripheral Component Interconnect bus transaction.” Under Petitioner’s construction, the claims would read on a bus transaction that complies with Peripheral Component Interconnect standard as well as virtually any other bus protocol that allows communication with a peripheral device. Petitioner’s construction improperly reads the “Peripheral Component Interconnect” limitation out of the claim.

An example using an embodiment in the ’814 patent illustrates how overbroad Petitioner’s proposed construction is. In connection with Figure 4, the ’814 patent describes an IDE bus. (*See* Ex. 1001, at 7:19-29.) Even though an IDE bus and a PCI bus are different types of buses, under Petitioner’s broad construction a transaction on an IDE bus would meet the limitation. In particular, an IDE bus complies with a different bus protocol that formats transactions different from a PCI bus for peripheral component communication. For example, the ’814 patent calls for a separate IDE controller to generate transactions particular to the IDE bus, not PCI bus transactions, for a disk drive peripheral

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component: “IDE controller 429 generally supports and provides timing signals necessary for the IDE bus.” (Ex. 1001, at 7:23-25.)

The specification also groups the PCI bus separately from the IDE bus and other buses. It notes that additional bus protocols could replace the IDE bus, lumping them all together, but does not include PCI: “In the present embodiment, the IDE controller is embodied as a 643U2 PCI-to IDE chip from CMD Technology, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, USB, and the like in alternative embodiments of the present invention.” (Ex. 1001, at 7:25-29.)

Even though the specification differentiates PCI from the other bus protocols, any bus in accordance with those other bus protocols could potentially meet the limitation under Petitioner’s construction. Petitioner’s construction is inconsistent with the specification and the express definition in the claims and should be rejected.

2. Petitioner offers insufficient evidence and explanation for its unreasonably broad construction

The only evidence Petitioner cites to support its construction is a *Markman* order from an earlier litigation announcing it. (Petition, at 13.) After summarizing Judge Davis’ findings from the *Markman* order, Petitioner repeats the construction. (*Id.*) Yet, Petitioner does not (1) explain why the Board should adhere to the

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district court's construction, (2) identify any portion of the specification supporting it, or (3) offer any expert testimony as to its validity. (*Id.*) Petitioner simply fails to backup its proposed construction. (*Id.*) A construction that ignores such basic tenants of patent law must be rejected. *See DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) ("In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.") (citations omitted)).

Finally, in the current related district court, Petitioner agrees that the *Markman* order it relies on here improperly construed PCI bus. (Ex. 2006, at 1.) In the district court, Petitioner proposed that "PCI bus transaction" should be construed in accordance with the PCI protocol standard. (*Id.* at 1, 3-8.) Over the course of several pages, Petitioner cited evidence and testimony from the intrinsic and extrinsic record to support its construction. (*Id.*) Even though a different claim construction standard applies there, Petitioner's plainly inconsistent position on the meaning of "PCI" and "PCI bus transaction" highlights just how overbroad its construction is here. Petitioner cited to the specification the '814 patent, the specification and prosecution history of related patents, art cited on the face of the '814 patent, deposition testimony, and other extrinsic evidence. Indeed, Petitioner cited to some of the same evidence Patent Owner relies on for its claim

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construction here, including the same embodiment descriptions in the '814 patent (Ex. 2006, at 4) and the PCI Local Bus Specification (Ex. 2006, at 7). Yet, of all the pages of support it cited for its district court construction, Petitioner cites nothing that suggests that "PCI" be read out of the Petitioned Claims. Petitioner's flawed and inconsistent construction should be rejected.

III. INSTITUTION ON GROUNDS 3-6 SHOULD BE DENIED BECAUSE THE BOGAERTS DRAFT IS NOT A "PRINTED PUBLICATION" UNDER 35 U.S.C. § 102(B)

Petitioner relies on Bogaerts et al., *RD24 Status Report: Application of the Scalable Coherent Interface to Data Acquisition at LHC* ("the Bogaerts Draft") (Ex. 1011), for Grounds 3-6. According to Petitioner, the Bogaerts Draft is a prior art printed publication under § 102(b). (Petition, at 58.) Whether the Bogaerts Draft is a prior art printed publication under § 102(b) depends on "the facts and circumstances surrounding its disclosure to members of the public." *Samsung Electronics Co. Ltd. v. Rembrandt Wireless Technologies, L.P.*, IPR2014-00514, Paper 18, at 6 (PTAB Sept. 9, 2014) (citing *In re Klopfenstein*, 380 F.3d 1345, 1350 (Fed. Cir. 2004)). To establish that the Bogaerts Draft was a printed publication, Petitioner has the burden show that the document was "sufficiently accessible to the public interested in the art." *See In re Lister*, 583 F.3d 1307, 1311 (Fed. Cir. 2009); *Samsung Electronics*, IPR2014-00514, Paper 18, at 9-10 (PTAB Sept. 9, 2014) (finding that Petitioner did not make a "sufficient showing"

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that a document was a printed publication). To qualify a reference as a printed publication, Petitioner must submit “sufficient proof of its dissemination or that it has otherwise been available and accessible to persons concerned with the art to which the document relates and thus most likely to avail themselves of its contents.” *In re Wyer*, 655 F.2d 221, 227 (CCPA 1981).

Petitioner asserts that the Bogaerts Draft is a prior art printed publication based solely on an October 2, 1996 date printed on its first page. (Petition, at 11, 58.) Aside from pointing to the October 1996 date, Petitioner provides no evidence or explanation of the Bogaerts Draft’s public accessibility. (*Id.*) And the October 1996 exhibits none of the indicia typically associated with a publication date. A date on the face of a draft document like the Bogaerts Draft is just as likely an edit date or an internal circulation date, not a publication or copyright date that might be found on a journal article or publicly disseminated paper. As a result, Petitioner fails to meet its burden to show public accessibility. In fact, evidence from the CERN document server indicates that the Bogaerts Draft was inaccessible until 2008. (Ex. 2004, at 1.) The Bogaerts Draft is not a prior art printed publication, and Institution of Grounds 3-6, which rely on the Bogaerts Draft, should be denied. *Samsung Electronics*, IPR2014-00514, Paper 18, at 9-10 (PTAB Sept. 9, 2014).

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A. The Bogaerts Draft Is An Internal Draft Report Unavailable to Persons of Ordinary Skill

The Bogaerts Draft on its face is a draft status report internal to a CERN project team. As shown in the excerpted image from the Bogaerts Draft below, the authors titled it “preliminary.” (Ex. 1011, at 1.) In other words, the Bogaerts Draft was not final; it was not publication-ready. According to the authors, the Bogaerts Draft was a preliminary draft to be further revised because the project was incomplete. (Ex. 1011, at 1 (noting the draft would be revised for “the next LBC meeting” because of “incomplete milestone measurements due to delay in delivery of SCI equipment”).) There is simply no indication that it was disseminated to the public or distributed or made available beyond the co-authors in October 1996.

**Figure 1 - Page 1 excerpted from the Bogaerts Draft
(Ex. 2012, at 1)**

EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH
This status report is preliminary¹ and will be revised for the next LCB meeting

1. incomplete milestone measurements due to delay in delivery of SCI equipment

The only evidence Petitioner identifies to support its contention that the Bogaerts Draft is prior art is the date on its face, October 2, 1996. (Petition, at 11, 58.) Neither Petitioner nor the Bogaerts Draft explains the meaning of the October

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1996 date. It is unclear whether the date is the date the document was saved the last time, an intermediate edit date, or the date it was circulated among the authors or others at CERN. With such uncertainty about the meaning of the October 1996 date, Petitioner has not met its burden to establish the Bogaerts Draft as prior art. *Samsung Electronics*, IPR2014-00514, Paper 18, at 9-10 (PTAB Sept. 9, 2014) (finding that Petitioner did not make a “sufficient showing” of dissemination outside of working group to establish that a document was a printed publication).

The October 1996 date is not the kind of designated copyright or publication date typically relied on to show publication. *See, e.g., ZTE Corporation v. IPR Licensing, Inc.*, IPR2014-00525, Paper 19, at 16 (PTAB Sept. 17, 2014) (finding that a copyright date on a European Telecommunications Standards Institute paper reasonably suggested publication); *IBM v. Intellectual Ventures II LLC*, IPR2014-00681, Paper 11, at 13-14 (PTAB Oct. 30, 2014) (finding a threshold showing that a product brochure was prior art based on its copyright date). Nothing about the October 1996 date suggests publication, particularly when viewed in context with the authors’ statements on the face of the Bogaerts Draft that suggest it was a draft internal status report.

If the Bogaerts Draft were truly prior art, then Petitioner could have used the well-known techniques for proving documents were publicly available. For example, Petitioner could have submitted an affidavit from one of the authors

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addressing public distribution of the draft or an affidavit from a librarian at CERN or some other library to confirm the date of indexing for the library collection.

See, e.g., Finisar Corp. v. Thomas Swan & Co. Ltd., IPR2014-00460, Paper 9, at 16, 19 (PTAB Aug. 21, 2014) (finding a sufficient showing that a document was prior art based on librarian testimony that document was indexed and shelved).

Alternatively, Petitioner could have submitted expert testimony about public accessibility of CERN draft documents generally or the meaning of dates on CERN draft documents. *See, e.g., Rackspace US, Inc. v. PersonalWeb*

Technologies, LLC, IPR2014-00059, Paper 9, at 33-34 (PTAB Apr. 15, 2014) (crediting expert testimony about the availability of a reference on a newsgroup).

Petitioner simply offers no evidence or testimony to support its claim that the Bogaerts Draft was publicly accessible as of October 1996. (Petition, at 11, 58.)

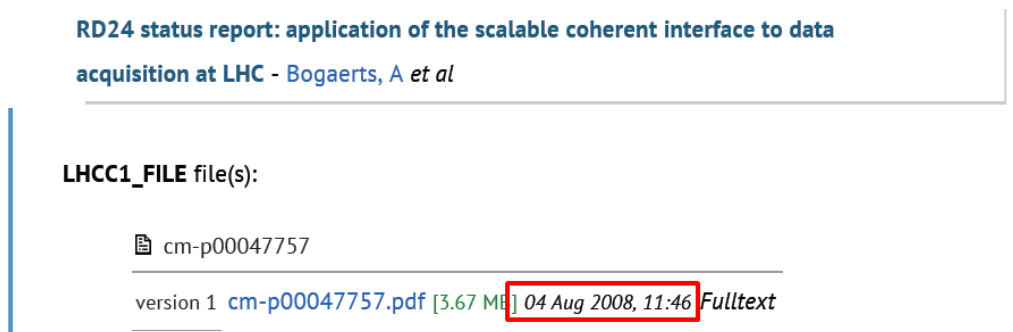
At the very least, in the absence of evidence, Petitioner could have explained the Bogaerts Draft's availability or how a person of ordinary skill in the art could have obtained a copy with reasonable diligence. *See EMC Corp. v. PersonalWeb Technologies, LLC*, IPR2013-00084, Paper, at 18-22 (PTAB May 17, 2013) (finding that a reference qualified as prior art because petitioner explained how the document was available as of the document's date). Petitioner failed even to offer attorney argument to show the Bogaerts Draft is prior art as of October 1996.

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In short, Petitioner offers no support or explanation showing the Bogaerts Draft was a printed publication available to persons of skill in the art. To the contrary, the document suggests on its face that it was an unpublished internal draft. For at least this reason, the Board should deny institution on Grounds 3-6 which rely on the Bogaerts Draft. *Kyocera Wireless Corp. v. ITC*, 545 F.3d 1340, 1350 (Fed. Cir. 2008) (“A reference is publicly accessible upon a satisfactory showing that it was disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate it.” (internal citation and quotation marks omitted)).

B. Evidence from CERN Suggests the Bogaerts Draft Was Not Available Until 2008

Aside from the authors’ description of the Bogaerts Draft as a preliminary document, other evidence affirmatively shows that it was not published until 2008. The current CERN library document server indicates that the Bogaerts Draft was posted on August 4, 2008, long after the effective filing date of the ’814 patent:



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(Ex. 2004 (annotated).)

The August 2008 date is the only evidence of a publication date for the Bogaerts Draft. CERN publishes articles, books, papers, and other documents on its document server through the CERN library and through the CERN document server in particular. (Ex. 2005, at 1.) By making documents available to the public through the document server, the August 2008 on the listing for the Bogaerts Draft on the document server is a more reliable indicator of its publication date than the unlabeled October 1996 date on its face. In short, it is more likely than not that the Bogaerts Draft was not published until at least 2008. Petitioner has failed to show by preponderance of the evidence that the Bogaerts Draft was prior art as of October 1996. Institution on Grounds 3-6, which rely on the Bogaerts Draft, should be denied.

IV. INSTITUTION ON GROUNDS 1-6 SHOULD BE DENIED BECAUSE THE OBVIOUSNESS COMBINATIONS LACK SUFFICIENT RATIONALE

A petition must identify with particularity the grounds on which the challenge to each claim is based. 35 U.S.C. § 312(a)(3). Under 37 C.F.R. § 42.22(a), a petition must include a statement of the precise relief requested and, under 37 C.F.R. § 42.104, the burden is on the petitioner to establish “[h]ow the construed claim is unpatentable” by specifying “where each element of the claim is found in the prior art patents or printed publications relied upon.” Petitioner failed

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to meet its burden for Grounds 1-6 for particular claims because it asserts numerous combinations in the alternative without specifying which combinations should be instituted. Petitioner's failure to meet its burden to establish the grounds of unpatentability by not specifying the asserted combinations affects the following grounds and claims:

- Ground 1 for claims 24
- Ground 2 for claim 32
- Ground 3 for all Petitioned Claims
- Grounds 4-6 for all Petitioned Claims

Petitioner also failed to meet its burden because it does not explain how a person of ordinary skill in the art would combine references, affecting the following grounds and claims:

- Ground 1 for claims 24 and 32
- Ground 2 for claim 32
- Ground 3 for all Petitioned Claims
- Grounds 4-6 for all Petitioned Claims

Petitioner's shotgun approach to its obviousness combinations lacks sufficient analysis. Grounds 1-6 for the above claims should therefore be denied. *See, e.g., Edmund Optics, Inc. v. Semrock, Inc.*, IPR2014-00583, Paper 9, at 10-12 (PTAB Sept. 19, 2014) (denying institution because petitioner offered

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combinations of references in the alternative); *Wowza Media Systems, LLC v.*

Adobe Systems Inc., IPR2013-00054, Paper 12, at 10-11 (PTAB Apr. 8, 2013)

(refusing to consider undeveloped unpatentability theories).

A. For Each of Grounds 1-6, Petitioner Fails to Specify Which of Its Alternative Combinations It Asserts

For Grounds 1-6, Petitioner asserts at least 16 different combinations using the following seven references.

Table 3 – List of References potentially cited in Grounds 1-6

Reference	Exhibit Number
U.S. Patent No. 5,608,608 (“Flint”)	1002
Horst, TNet: A Reliable System Area Network (“Horst”)	1009
U.S. Patent No. 6,148,357 (“Gulick”)	1010
Bogaerts, Application of the Scalable Coherent Interface to Data Acquisition at LHC (“Bogaerts Draft”)	1011
U.S. Patent No. 6,012,145 (“Mathers”)	1014
U.S. Patent No. 5,961,623 (“James”)	1018
LVDS Owner’s Manual	1019

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As explained in further detail below, Petitioner asserts the combinations in the alternative, failing to specify which combinations constitute which grounds. The Board has found similar petitions insufficient where a petitioner asserts combinations in the alternative, tries to reserve the ability to assert different alternative combinations, or fails to specify with particularity the asserted combination. For example, the Board has refused to consider combinations that a petitioner has argued could be an alternative ground but that were not specifically identified. *Apple Inc. v. Achates Reference Publishing, Inc.*, IPR2013-00081, Paper 21, at 20-21 (PTAB June 3, 2013).

In IPR2013-00054, the Board refused to consider numerous alternative combinations from the petition. The Board found that the Petitioner failed to “explain how the references to be applied in the alternative might remedy the deficiencies in the other references, [or apply] the references as proposed to be combined in the alternative against any specific claims.” *Wowza Media Systems, LLC v. Adobe Systems Inc.*, IPR2013-00054, Paper 12, at 10-11 (PTAB Apr. 8, 2013).

Additionally, in IPR2014-00583, the Board denied institution where the petitioner had characterized grounds using “multiple conjunctive and disjunctive ‘and/or’ connectors” to increase the number of potential combinations. *Edmund*

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Optics, Inc. v. Semrock, Inc., IPR2014-00583, Paper 9, at 10-12 (PTAB Sept. 19, 2014).

Like the petitioners in those cases, Petitioner offers alternative combinations, fails to specify which of the combinations should be instituted, and fails to explain how the combinations should be applied. Accordingly, institution of Ground 1 for claim 24, Ground 2 for claim 32, and Grounds 3-6 for all Petitioned Claims should be denied.

**1. Ground 1 should not be instituted on claim 24 because
Petitioner does not specify which combination it asserts**

Claim 24 recites a “main memory coupled to said microprocessor unit through said north bridge.” (Ex. 1001, 27:30-31.) In its attack on claim 24 for Ground 1, Petitioner relies on three references: Flint, Gulick, and Mathers. (Petition, at 19.) Specifically for the limitation above, Petitioner relies just on Flint and Gulick. In particular, Petitioner asserts two different theories to disclose this limitation, contending that (1) the limitation would have been an obvious design choice for Flint based on the knowledge of a person of ordinary skill and (2) the limitation would have been obvious based on Flint in combination with Gulick. (Petition, at 21-22.) Thus, Ground 1 results in the following potential unpatentability theories:

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Table 4 – Potential Combinations for Ground 1

Combination	Potential Combinations
1	Flint + Mathers
2	Flint + Mathers + Gulick

Petitioner fails to explain which of the two potential combinations constitutes Ground 1—or even if both combinations make up Ground 1. (*See* Petition, at 19, 21-22.) By failing to specify which unpatentability theory it asserts and, thus, multiplying the potential asserted combinations, Petitioner has failed to meet its burden to identify with particularity the ground of unpatentability for Ground 1 and Ground 1 against claim 24 should not be instituted. *See Edmund Optics*, IPR2014-00583, Paper 9, at 10-12 (PTAB Sept. 19, 2014) (denying institution on alternate combinations); *Wowza Media Systems*, IPR2013-00054, Paper 12, at 10-11 (PTAB Apr. 8, 2013) (denying institutions for failure to specify with particularity the asserted combinations).

**2. Ground 2 should not be instituted on claim 32 because
Petitioner does not specify which combination it asserts**

Ground 2 creates two more alternative combinations using the Horst and Mathers references. (Petition, at 35.) Claim 32 requires the mass memory storage of claim 31 to comprise a flash memory. (Ex. 1001, at 28:44-45.) Petitioner argues in the alternative that (1) Horst inherently discloses a flash memory as

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required by claim 32 (Petition, at 35 (“a flash memory is inherently disclosed in Horst”) and (2) Mathers discloses a flash memory and would be combined with Horst (*Id.*). Thus, for claim 32, Petitioner asserts the following combinations in the alternative:

Table 5 – Potential Combinations for Claim 32 of Ground 2

Combination	Potential Combinations
3	Horst alone
4	Horst + Mathers

Again, each of the combinations is an alternative theory, and Petitioner does not explain which alternative combination constitutes its Ground 2 theory for claim 32 or if both combinations together make up its theory. (Petition, at 35.)

Petitioner leaves the asserted combination open ended and, therefore, institution on Ground 2 against claim 32 should be denied. *See Edmund Optics*, IPR2014-00583, Paper 9, at 10-12 (PTAB Sept. 19, 2014) (denying institution on alternate combinations); *Wowza Media Systems*, IPR2013-00054, Paper 12, at 10-11 (PTAB Apr. 8, 2013) (denying institutions for failure to specify with particularity the asserted combinations).

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3. Ground 3 should not be instituted because Petitioner does not specify which combination it asserts

For Ground 3, Petitioner asserts four different theories, contending that the Bogaerts Draft in combination with Mathers and in some further combination with James and Gulick renders claims the Petitioned Claims obvious. (Petition, at 38, 40-45, 48.) Thus, Ground 3 results in the following potential unpatentability theories:

Table 6 – Potential Combinations for Ground 3

Combination	Potential Combinations
5	Bogaerts Draft + Mathers
6	Bogaerts Draft + Mathers + James
7	Bogaerts Draft + Mathers + Gulick
8	Bogaerts Draft + Mathers + James + Gulick

Claim 24 recites a “north bridge directly coupled to said microprocessor unit” and claim 31 recites “a peripheral bridge coupled to said microprocessor unit without any intervening Peripheral Component Interconnect (PCI) bus.” (Ex. 1001, at 27:30-31, 28:34-36.) Petitioner asserts that each of the Bogaerts Draft, James, and Gulick disclose these limitations. (Petition, at 40-44.) But Petitioner does not limit Ground 3 to any one of the combinations. (*Id.*) Thus, Petitioner

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argues, in the alternative, that the four combinations make up Ground 3. By failing to specify which unpatentability theory it asserts and, thus, multiplying the potential asserted combinations, Petitioner has failed to meet its burden to identify with particularity the ground of unpatentability for Ground 3 and Ground 3 should not be instituted. *See Edmund Optics*, IPR2014-00583, Paper 9, at 10-12 (PTAB Sept. 19, 2014) (denying institution on alternate combinations); *Wowza Media Systems*, IPR2013-00054, Paper 12, at 10-11 (PTAB Apr. 8, 2013) (denying institutions for failure to specify with particularity the asserted combinations).

4. Grounds 4-6 should not be instituted because Petitioner does not specify which combinations it asserts

For Grounds 4-6, Petitioner combines LVDS Owner's Manual with every potential combination of Grounds 1-3 to create at least another eight additional combinations. (Petition, at 51-52.) Once again, Petitioner does not say which of the combinations it actually asserts or if it intends to rely on all eight combinations.

Table 7 – Potential Combinations for Grounds 4-6

Combination	Potential Combinations
9	Flint + Mathers + LVDS Owner's Manual
10	Flint + Mathers + Gulick + LVDS Owner's Manual
11	Horst alone + LVDS Owner's Manual

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Combination	Potential Combinations
12	Horst + Mathers + LVDS Owner's Manual (claim 32)
13	Bogaerts Draft + Mathers + LVDS Owner's Manual (claim 32)
14	Bogaerts Draft + Mathers + James + LVDS Owner's Manual
15	Bogaerts Draft + Mathers + Gulick + LVDS Owner's Manual
16	Bogaerts Draft + Mathers + James + Gulick + LVDS Owner's Manual

Adding LVDS Owner's Manual to Grounds 1-3 to make up Grounds 4-6 simply doubles the number of additional potential alternative grounds. Petitioner again does not limit the combinations, vaguely arguing that a "skilled artisan at the time would been motivated to apply the teachings in LVDS Owner's Manual to any computer bus system." (Petition, at 52.) Based on Petitioner's addition of another eight potential combinations with no explanation for Grounds 4-6, institution of Grounds 4-6 should be denied. *See Edmund Optics*, IPR2014-00583, Paper 9, at 10-12 (PTAB Sept. 19, 2014) (denying institution on alternate combinations); *Wowza Media Systems*, IPR2013-00054, Paper 12, at 10-11 (PTAB

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Apr. 8, 2013) (denying institutions for failure to specify with particularity the asserted combinations).

B. For Each Possible Combination of Grounds 1-6, Petitioner Omits a Rational Underpinning for How References Would Be Combined

Another reason for denying institution on Ground 1 for claims 24 and 32, Ground 2 for claim 32, and Grounds 3-6 for all Petitioned Claims is Petitioner's failure to address how or why any of its secondary references is combined with any other reference. To meet its burden to establish a reasonable likelihood of success on each of Grounds 1-6, Petitioner must have provided some "rational underpinning" for each combination of those grounds. *See In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (holding that "there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness"). A "rational underpinning" requires that Petitioner explain how or why a reference would be combined with another reference. *Lake Cable, LLC v. Windy City Wire Cable and Tech. Prods., LLC*, IPR2013-00528, Paper 11, at 18-19, 24-25, 26-27 (PTAB Feb. 19, 2014) (denying institution based on petitioner's failure to explain why or how a person of ordinary skill in the art would combine references and how asserted combinations would result in the stated advantages).

For potential combinations of Grounds 1-6, Petitioner offers boilerplate obviousness conclusions and omits a rational underpinning for how references

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would be combined. As discussed further in the sections below, neither Petitioner nor Petitioner's expert explains how or whether a person of ordinary skill would find it obvious that the teachings of a secondary reference should be added to or substituted for the teachings of another reference. And Petitioner and Petitioner's expert ignore whether references include overlapping or contradictory disclosures. Petitioner leaves the Board and the Patent Owner to guess at the rationale for all of the potential combinations and how Petitioner proposes a person of ordinary skill would cobble together the references. Petitioner offers no rational underpinning and, thus, fails to establish a reasonable likelihood of success of proving the Petitioned Claims would have been obvious under Grounds 1-6. *Lake Cable, LLC v. Windy City Wire Cable and Tech. Prods., LLC*, IPR2013-00528, Paper 11, at 18-19, 24-25, 26-27 (PTAB Feb. 19, 2014). Institution of Grounds 1-6 should be denied.

1. For Ground 1, Petitioner does not explain how a person of ordinary skill would combine Flint and Gulick to meet the requirements of claim 24

For Ground 1, Petitioner asserts two alternative combinations involving Flint and Gulick to render claim 24 obvious. (Petition, at 19, 21-22.) Petitioner asserts that both Flint and Gulick disclose the "main memory coupled to said microprocessor unit through said north bridge" limitation of claim 24. (Petition, at 21-22.) In particular, Petitioner asserts that the above limitation (1) would have

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been an obvious design choice for Flint based on the knowledge of a person of ordinary skill and (2) would have been obvious based on Flint in combination with Gulick. (Petition, at 21-22.)

For the first theory based solely on Flint, Petitioner claims that a skilled artisan “in October of 1998 would known that memory could be tied to a north bridge chip or directly into the processor bus and would have chosen coupling through the north bridge to simplify the board layout, reduce electromagnetic interference and save space.” (Petition, at 22.) For this theory, Petitioner cites to no facts to support either the suggestion that “memory could be tied to a north bridge chip or directly into the processor bus” or that a skilled artisan would have chosen to couple a memory to a north bridge chip “to simplify the board layout, reduce electromagnetic interference and save space.” (*See id.*) Rather, Petitioner relies solely on unsubstantiated assertions. Petitioner cites only to expert testimony that, itself, is unsubstantiated. (Ex. 1003, ¶¶ 56, 118, 140[24C(iii)].) And as for Petitioner’s stated motivation specifically, Petitioner’s expert declaration merely parrots the words in the petition. (Ex. 1003, ¶¶ 118, 140[24C(iii)] (“it would simplify the board layout, reduce electromagnetic interference, and save space”).)

In short, Petitioner’s rationale that modifying Flint based on the knowledge of a skilled artisan so that its “main memory [was] coupled to said microprocessor

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unit through said north bridge” as required by claim 24 is nothing more than unsubstantiated assertion. Accordingly, Ground 1 against claim 24 based on Petitioner’s first theory should not be instituted. *TRW Automotive US LLC v. Magna Electronics, Inc.*, IPR2014-00251, Paper 19, at 5 (PTAB July 31, 2014) (holding that “[t]he mere possibility of [a limitation in a claim] . . . is not sufficient to render the [limitation] obvious”); *Veeam Software Corp. v. Symantec Corp.*, IPR2013-00145, Paper 12, at 11-12 (PTAB Aug. 7, 2013) (denying institution after finding “arguments and declaration amount to little more than unsubstantiated assertions about the combinability [of art], the manner of . . . combination, and the results thereby obtained”).

For the second theory based on a combination of Flint and Gulick, Petitioner provides a virtually identical rationale as it provides for the first theory based solely on Flint. Petitioner states:

A skilled artisan would have been motivated to combine the teachings of Flint with Gulick to integrate the memory controller in the north bridge as taught by Gulick to reduce the number of components in the system, simplifying the system design and reducing cost, as well as to improve performance and reduce electromagnetic inference.

(Petition, at 22.)

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Again, Petitioner's argument is nothing more than unsubstantiated assertions. The only support Petitioner cites is its expert declaration which, again, is unsupported by any facts. (Ex. 1003, ¶ 131, 140[24C(iii)].) Accordingly, Petitioner fails to meet its burden to show a reasonable likelihood of success on its second theory combining Flint and Horst. Ground 1 against claim 24 under Petitioner's second theory combining Flint and Horst should not be instituted. *TRW Automotive*, IPR2014-00251, Paper 19, at 5 (PTAB July 31, 2014); *Veeam Software*, IPR2013-00145, Paper 12, at 11-12 (PTAB Aug. 7, 2013).

2. For Ground 1, Petitioner does not explain how a person of ordinary skill would combine Flint and Mathers to meet the requirements of claim 32

For Ground 1, Petitioner asserts two alternative combinations involving Flint and Mathers to render claim 32 obvious. (Petition, at 26-27.) Petitioner asserts that both Flint and Mathers disclose "wherein said mass memory storage device comprises a flash memory" as required by claim 32. (Petition, at 26-27.) In particular, Petitioner asserts that the above limitation (1) is inherent in Flint and (2) would have been obvious based on Flint in combination with Mathers. (Petition, at 26-27.)

Petitioner's rationale for combining Flint and Mathers does not take into account that both references allegedly disclose the flash memory required by claim 32 and, thus, have overlapping disclosure. Petitioner does not identify any missing

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or deficient disclosure in Flint that Mathers remedies. (*See* Petition, at 26-27.)

Petitioner also does not state whether a person of ordinary skill would find it obvious to substitute Mathers' flash memory for Flint's flash memory or other memory device or add Mather's flash memory to Flint. (*See id.*)

Petitioner also does not provide the required support for the alleged motivations to combine. According to Petitioner, "there is a strong motivation to combine [Mathers with Flint] because flash memory is faster, more compact, uses less power and is less prone to damage compared to traditional hard disk drives." (Petition, at 35.) But Petitioner does not explain how adding flash memory to Flint results in those benefits. (*See id.*) Furthermore, Petitioner does not explain how adding flash memory to Horst would have made Horst's system more compact, consume less power, and be less prone to damage. (*See id.*) Indeed, adding flash memory, another component, to Flint would seem to *enlarge* Flint's module and require additional circuitry that, in turn, called for more power consumption.

In short, Petitioner fails to explain how or why a person of ordinary skill would combine Flint and Mathers the required specificity. Petitioner thus fails to meet its burden to show a reasonable likelihood of success on Ground 1 against claim 32 and institution of Ground 1 for claim 32 should be denied. *See In re Kahn*, 441 F.3d at 988 (Fed. Cir. 2006); *Lake Cable*, IPR2013-00528, Paper 11, at 18-19, 24-25, 26-27 (PTAB Feb. 19, 2014).

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3. For Ground 2, Petitioner does not explain how a person of ordinary skill would combine Horst and Mathers to meet the requirements of claim 32

For Ground 2, Petitioner asserts another two alternative combinations to render claim 32 obvious. Here, the combinations involve Horst and Mathers. (Petition, at 35.) Petitioner asserts that both Horst and Mathers disclose “wherein said mass memory storage device comprises a flash memory” as required by claim 32. (*Id.*) In particular, Petitioner asserts that the above limitation (1) is inherent in Horst and (2) would have been obvious based on Horst in combination with Mathers. (*Id.*)

Petitioner’s rationale for combining Horst and Mathers does not take into account that both references allegedly disclose the flash memory required by claim 32 and, thus, have overlapping disclosure. Petitioner does not identify any missing or deficient disclosure in Horst that is remedied by Mathers. (*See* Petition, at 35.) Petitioner also does not state whether a person of ordinary skill would find it obvious to substitute a Mathers’ flash memory for Horst’s or add Mather’s flash memory to Horst. (*See id.*)

Moreover, assuming that Horst actually does not inherently disclose flash memory, Petitioner does not address whether Horst could accommodate a flash memory without any additional modification. (*See id.*) After all, Horst was a new and proprietary architecture, not a standard system. (*See* Ex. 1009, at 1 (“A major

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departure from traditional I/O systems, TNet is a new system area network”).)

Given that Horst’s TNet included a new and allegedly faster proprietary bus standard and architecture (*See* Petition, at 28-29), a person of ordinary skill in the art may not have understood that a TNET module would accommodate a flash memory.

Petitioner also fails to address where or how a person of ordinary skill would add a flash memory to Horst. (*See* Petition, at 35.) Mathers discloses a particular type of non-volatile EPROM flash memory on a “disk drive electronics board” as part of a portable disk drive. (Ex. 1014, at Abstract, 1:58-61.) But Petitioner does not identify a “disk drive electronics board” in Horst. (*See* Petition, at 35.)

And Petitioner does not reconcile apparent inconsistencies in Horst’s and Mathers’ disclosures. For example, Horst’s system was directed to I/O for database systems (Ex. 1009, at 3 (“connecting all I/O devices . . . supports either shared-disk or shared-nothing database systems.”)) and, thus a person of ordinary skill would likely understand that Horst’s disks were large and both readable and writable. In contrast, Mathers’ flash memory was small and non-volatile (i.e., not writable). (Ex. 1014, at 3:46-59 (“As can be seen from FIGS. 1, 2 and 3, IC5 is a non-volatile flash EPROM (e.g. ATMEL AT29C512 (64K bytes) in a 32 pin TSOP package) constituting a first memory means.”).) Petitioner does not explain why a person of ordinary skill in the art would replace Horst’s I/O disks with such a small

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read-only memory device as Mathers' flash memory. (*See* Petition, at 35.)

Petitioner leaves the Board and Patent Owner to guess as to how the technology in Mathers might apply to Horst and how any resulting combination might look.

Petitioner also does not provide the required support for the alleged motivations to combine. According to Petitioner, "there is a strong motivation to combine [Mathers with Horst] because flash memory is faster, more compact, uses less power and is less prone to damage compared to traditional hard disk drives." (Petition, at 35.) But Petitioner does not explain how adding flash memory to Horst results in those benefits. (*See id.*) Horst claims, and Petitioner agrees, that the Horst's I/O was already faster than other systems. (*Id.* at 29; Ex. 1009, at 1.) Petitioner does not explain how adding flash would improve the speed of a system that was custom designed to already be faster. (*See* Petition, at 35.) Furthermore, Petitioner does not explain how adding flash memory to Horst would have made Horst's system more compact, consume less power, and be less prone to damage. (*See id.*) Indeed, adding flash memory, another component, to Horst would seem to *enlarge* Horst and require additional circuitry that, in turn, called for more power consumption.

In short, Petitioner fails to explain how or why a person of ordinary skill would combine Horst and Mathers the required specificity. Petitioner thus fails to meet its burden to show a reasonable likelihood of success on Ground 2 against

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claim 32 and institution of Ground 2 on claim 32 should be denied. *See In re Kahn*, 441 F.3d at 988 (Fed. Cir. 2006); *Lake Cable*, IPR2013-00528, Paper 11, at 18-19, 24-25, 26-27 (PTAB Feb. 19, 2014).

4. For Ground 3, Petitioner does not explain how a person of ordinary skill would combine the Bogaerts Draft, James, and Gulick

For Ground 3, Petitioner asserts four possible combinations involving the Bogaerts Draft, James, and Gulick. (Petition, at 39; *see also* Ex. 1003, at ¶ 160.)

Petitioner asserts that all three references disclose the following two elements:

- (1) **From claim 24:** “north bridge directly coupled to said microprocessor unit” (Petition, at 40-45.)
- (2) **From claim 31:** “a peripheral bridge coupled to said microprocessor unit without nay intervening Peripheral Component Interconnect (PCI) bus.” (Petition, at 40-45.)

Petitioner’s stated motivation for combining the Bogaerts Draft with James for both claims 54 and 60 is that “James states that SerialExpress is the next iteration of the IEEE 1596 SCI standard.” (Petition, at 42.) For the Bogaerts Draft and Gulick combination for both claims, Petitioner argues that a skilled artisan would be motivated to combine the references “to have better (faster) access to the processor bus as taught by Gulick.” (*Id.* at 45.) Petitioner offers no explanation

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for why a person of ordinary skill would combine all three of the Bogaerts Draft, James, and Gulick. (*See id.*)

Petitioner’s rationale for the combinations does not take into account that all three references allegedly fully disclose the above elements and, thus, have overlapping disclosure. Petitioner does not identify any missing or deficient disclosure in any of the three references with respect to the elements. (*See* Petition, at 40-45.) Petitioner also does not state whether a person of ordinary skill would find it obvious to substitute a portion of one of the references for a portion of another references or whether a person of ordinary skill would find it obvious to simply add some portion of one of the references to another. (*See id.*) For example, Petitioner does not explain whether a person of ordinary skill would modify the Bogaerts Draft’s architecture to directly couple a north bridge or peripheral bridge to a microprocessor in an identical way that James or Gulick allegedly do or even whether that would be possible. (*See id.*) Petitioner leaves the Board and Patent Owner to guess as to how the technology in James and Gulick might apply to the Bogaerts Draft and how any resulting combination might look.

Petitioner also does not provide any support for the alleged motivations to combine. For example, Petitioner states that “James states that SerialExpress is the next iteration of the IEEE 1596 SCI standard” but then fails to explain why that

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would provide motivation to an ordinary artisan to modify the Bogaerts Draft.

(Petition, at 42.) Petitioner does not explain in whether a next iteration of the the SCI standard would prompt a person of ordinary skill to replace the existing components in the Bogaerts Draft's system or even whether the next iteration would improve the function of the Bogaerts Draft's system. (*See id.*) In fact, the Bogaerts Draft was allegedly drafted *after* James was filed. (*Id.* at 58) And a person of ordinary skill was just as likely to understand that Bogaerts' version of the IEEE 1596 SCI is at least the same version of SCI in James, leaving a person of ordinary skill no reason to apply James to the Bogaerts Draft under Petitioner's rationale.

Petitioner's rationale for combining Gulick with Bogaerts is similarly insufficient. Petitioner claims that Gulick would provide "better (faster) access to the processor bus." (Petition, at 45.) But Petitioner does not identify *how* a person of ordinary skill would apply Gulick to the Bogaerts Draft to realize that benefit. (*See id.*) Moreover, Petitioner fails to support its assertion with any facts. For example, the Bogaerts Draft already claims fast access. (*E.g.*, Ex. 1010, at 4 ("The latency for memory accesses adds only a few microseconds to the equivalent access to local memory, even on PCI-SCI nodes which have no cache support.")). But Petitioner does not provide any support for the contention that Gulick is faster, or even better. (*See* Petition, at 45.)

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In short, Petitioner fails to explain how any of James, Gulick, or the Bogaerts Draft would be applied to remedy deficiencies of each other and does not explain why a person of ordinary skill would apply or substitute an element from one reference to another. Petitioner thus fails to meet its burden to show a reasonable likelihood of success on Ground 3. *See In re Kahn*, 441 F.3d at 988 (Fed. Cir. 2006); *Lake Cable*, IPR2013-00528, Paper 11, at 18-19, 24-25, 26-27 (PTAB Feb. 19, 2014).

5. For Ground 3, Petitioner does not explain how a person of ordinary skill would combine the Bogaerts Draft and Mathers to meet the requirements of claim 32

For Ground 2, Petitioner asserts that it would have been obvious to combine Mathers with the Bogaerts Draft to render claim 32 obvious. (Petition, at 49-50.) Petitioner offers an identical explanation for combining Mathers with the Bogaerts Draft as it offers for combining Mathers with Flint and Horst. (*Compare Id.* at 50 with *Id.* at 27, 35.) Specifically, Petitioner's entire rationale for combining Mathers with the Bogaerts Draft is the following:

Mathers discloses that the mass memory storage device may comprise a flash memory, and there is a strong motivation to combine this reference with Bogaerts because flash memory is faster, more compact, uses less power and is less prone to damage compared to traditional hard disk drives.

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(*Id.* at 50.)

Just as Petitioner failed to explain how a person of ordinary skill would combine Mathers with Flint or Horst, Petitioner also offers no explanation for how a person of ordinary skill would add Mathers' flash memory to the Bogaerts Draft's system. (*See Id.* at 50.) Again, Petitioner does not explain whether a person of ordinary skill would find it obvious to add Mathers' flash memory to the Bogaerts Draft or substitute to it in place of some existing component in the Bogaerts Draft. (*See id.*) And Petitioner fails to explain where in the Bogaerts Draft's system a person of ordinary skill would add Mathers' flash memory. (*See id.*) Additionally, Petitioner fails to explain with any specificity how a person of ordinary skill would realize any of the benefits through the a particular combination of Bogaerts Draft and Mathers. (*See id.*)

Petitioner's conclusory assertions lack the requisite rationale to explain the function of a Bogaerts Draft + Mathers combination. Petitioner thus fails to meet its burden to show a reasonable likelihood of success on Ground 3 against claim 32 and institution of Ground 3 for 32 should be denied. *See In re Kahn*, 441 F.3d at 988 (Fed. Cir. 2006); *Lake Cable*, IPR2013-00528, Paper 11, at 18-19, 24-25, 26-27 (PTAB Feb. 19, 2014).

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6. For Grounds 4-6, Petitioner does not explain how a person of ordinary skill would combine LVDS Owner's Manual with other references

For Grounds 4-6, Petitioner adds LVDS Owner's Manual to each combination from Grounds 1-4 resulting in eight additional combinations. Again, Petitioner provides no rationale for any of the additional potential combinations. Instead, Petitioner only concludes that any of the eight potential combinations involving LVDS Owner's Manual would have been obvious:

A skilled artisan at the time would have been motivated to apply the teachings in LVDS Owner's Manual to any computer bus system as a serial LVDS channel to keep up with the serialization trend with an affordable, easy solution, as described by the Manual. The motivation to combine is particularly strong given that LVDS channels are recommended for rack-mounted and box-to-box systems (such as with Horst and Bogaerts) or between a system and its peripherals (Flint).

(Petition, at 52 (citations omitted).)

Petitioner offers no explanation with any level of specificity how LVDS Owner's Manual could be combined with any other reference or any reasons specific to any of the references applying the LVDS Owner's Manual's teachings. (*See* Petition, at 52.) Petitioner offers no rational underpinning for the eight potential combinations of Grounds 4-6 and, therefore, institution should be denied.

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See In re Kahn, 441 F.3d at 988 (Fed. Cir. 2006); *Lake Cable*, IPR2013-00528, Paper 11, at 18-19, 24-25, 26-27 (PTAB Feb. 19, 2014).

V. CONCLUSION

Petitioner’s proposed construction of “PCI bus transaction” fails to account for important and limiting intrinsic and extrinsic evidence. Because Petitioner relies on its flawed construction of “PCI bus transaction” for each of the grounds, institution on Grounds 1-6 should be denied. Each of Grounds 3-6 should be denied institution for the additional reason that they rely on the Bogaerts Draft which is not prior art. Finally, Ground 1 for claims 24 and 32, Ground 2 for claim 32, and Grounds 3-6 for all Petitioned Claims are not supported with sufficient explanation or evidence; and therefore those grounds should be denied institution.

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CERTIFICATION OF SERVICE UNDER 37 C.F.R. §§ 42.6(e), 42.105(a))

I, Mark R. Schafer, hereby certify that on December 15, 2014 the foregoing
PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R.

§ 42.107, the associated Exhibit List, and all associated Exhibits were served
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